# RFIC's for Mobile Communication Systems Using SiGe Bipolar Technology

Rainer Götzfried, Frank Beißwanger, Stephan Gerlach, Andreas Schüppen, Harry Dietrich, Ulrich Seiler, Karl-Heinz Bach, and Jens Albers

***Abstract*—We report on design aspects and the implementation of RF integrated circuits (RFIC's) using TEMIC's SiGe heterojunction bipolar transistor (HBT) technology. SiGe HBT's with 50-GHz $f_T$ and $f_{\max}$ were obtained by a production process including polysilicon resistors, nitride capacitors, and spiral inductors showing $Q$ values up to 10. RF noise figures down to 1 dB at 2 GHz with an associated gain of 14-dB and 1-kHz $1/f$ corner frequency were obtained. The differences between the device parameters of Si bipolar junction transistor (BJT) and SiGe HBT technology and their influence on IC design are discussed. Design and measurement results of RFIC's, including a low-noise amplifier (LNA) and a power amplifier (PA) for application in a 1.9-GHz digital enhanced cordless telecommunications (DECT) RF front-end and 900-MHz preamplifier for a global system for mobile communication (GSM) power module are presented.**

***Index Terms*—Amplifier noise, bipolar integrated circuits, mobile communications, power amplifiers, silicon–germanium.**

## I. Introduction

MOBILE communication systems require low-cost RF front-end solutions for frequencies at or above 1 GHz. Advanced silicon technologies are starting to enter a market formerly occupied by GaAs FET technology. The advantages—beside the chip costs—are a higher integration level, which keeps system costs low, and good thermal conductivity, which is especially useful for power amplifier (PA) design. Also, the low leakage currents and the ability to integrate logic functions including power management makes the silicon technology attractive. The low noise figures required in such systems can be achieved by reducing base resistance and by increasing the current gain and the transit frequency of the device. One approach is the lateral downscaling of the conventional bipolar junction transistor (BJT) far below 1 $\mu$m [1], and another solution is the SiGe heterobipolar technology [2]–[4]. This technology provides high gain and low noise figures below 1 dB at 2 GHz without the need of sub-$\mu$ lithography and avoiding narrow emitter effects occurring on downscaled BJT's [1].

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## II. Comparison of the Key Design Parameters of Si BJT's and SiGe HBT's

From a designer's point of view, SiGe HBT's are very similar to Si BJT's. Basic principles gained in Si BJT circuits can, therefore, be applied to SiGe HBT circuit design in a straightforward manner. There are certainly several advantages of the SiGe technology.

1) For a given collector current density, SiGe HBT's require an input voltage $V_{BE}$ which is *lower* as compared to pure silicon bipolar technology. This holds particularly when the "true" heterojunction bipolar concept—in comparison with the drift transistor concept favored by other companies—is used. Due to the heterojunction effect, the collector current density is increased exponentially with the difference in bandgap between emitter and base, which is, in turn, proportional to the germanium content in the base. Although part of this gain is sacrificed to a base doping concentration which is 10–20 times higher compared to Si BJT technology, to achieve a given collector current density, an input voltage $V_{BE}$ is sufficient, which is about 80 mV lower compared to the Si BJT. This is especially useful when moving to lower supply voltages, as demanded by all mobile communication systems.
2) The SiGe heterojunction bipolar concept with inversion of the doping levels in emitter and base used in our process makes use of a lightly doped emitter layer. This drastically reduces base–emitter capacitance $C_{JE}$ and, therefore, high speed and high gain can be achieved at a lower current density, which is profitable to low-power design.
3) The high current gain achievable improves the input resistance and improves the low-noise properties in the input stages of low-noise amplifiers (LNA's).
4) Due to the high base-doping concentration, the base-width modulation by the base–collector voltage is less pronounced, leading to a higher early voltage as compared to Si BJT's. This allows for high output resistance of amplifier stages and the realization of very stable current sources.
5) Because of the high gain at frequencies above 2 GHz, a linearization by feedback is possible, which provides a good intermodulation behavior in PA's and LNA's.

The major disadvantage of silicon bipolar technology for communication systems is the low breakdown voltage, which

TABLE I
BREAKDOWN VOLTAGES FOR DIFFERENT SILICON TECHNOLOGIES

| Technology | $BV_{CE0}$ [V] | $BV_{CB0}$ [V] | $f_T$ [GHz] | $f_{max}$ [GHz] | @$V_{BC}$ [V] |
|---|---|---|---|---|---|
| Advanced Si-BJT [1] | 2.9 | 10 | 36 | 38 | 0 |
| SiGe-HBT from [4] | 2.5 | 9.9 | 61 | 74 | -1 |
| SiGe-HBT from [5] | 3.3 | – | 45 | 55 | -1 |
| SiGe-HBT from [6] | 5.3 | – | 28 | 57 | – |
| SiGe-HBT this work, with SIC | 3.5 | 9 | 50 | 50 | -2.2 |
| SiGe-HBT this work, no SIC | 6.0 | 13 | 30 | 55 | -2.2 |

makes the design of PA's a demanding task. The low breakdown voltage $BV_{CE0}$ is not a problem specific to SiGe, but is a problem of all advanced silicon bipolar processes, where the transit time is no longer determined by the base width, but by the width of the collector layer. The breakdown voltage is also the reason for the limitation of the current gain to the value of $\beta = 140$ in TEMIC's state-of-the-art technology, as a very high current gain worsens avalanche multiplication in the collector.

The problem is solved in TEMIC's technology by the use of two different n-p-n transistor types. The standard n-p-n uses a 450-nm collector layer doped to $2 \cdot 10^{16}$ cm$^{-3}$ with a collector–emitter breakdown voltage $BV_{CE0}$ of 6.0 V (see Table I). These devices are used, where only few transistors are arranged within $V_{CC}$, e.g., in the design of PA's. An additional mask step provides transistors with selective implantated collector (SIC). Due to the reduced collector width, those devices have higher gain and higher cutoff frequencies and are used when several transistors are cascaded. The breakdown voltage of those devices is $BV_{CE0} = 3.5$ V, which is still comparable with competing processes (see Table I).

## III. TECHNOLOGY

The SiGe HBT's were fabricated using TEMIC's bipolar production line. The process, which was recently described in [2], started with a buried layer formation and a channel-stop implantation on a 20 $\Omega \cdot$ cm substrate. The collector layers were formed by a 450-nm chemical vapor deposited (CVD) silicon deposition and seperated by a recessed LOCOS process. The collector contact regions were implanted with phosphorus. Subsequently, the CVD growth of the SiGe base followed. An implanted $\alpha$-Si emitter was deposited on top. The 21% Ge in the base and the $4{\cdot}10^{19}$ cm$^{-3}$ boron were kept constant. The SiGe growth is monocrystalline in the oxide windows and polycrystalline on the $SiO_2$. This process mainly differs from a conventional double poly self-aligned silicon bipolar technology by using the CVD–polysilicon as the base lead contact, i.e., the originally n-type top layer is converted to p by a $BF_2$ implantation. A selective implanted collector offers the possibility to build transistors with high breakdown voltage and low collector–base capacitance and on the same wafer HBT's with higher current densities and higher $f_T$, but higher capacitance and lower breakdown voltage. In order to reduce the lead and contact resistances of the emitter and the base, titanium silicide was formed by a salicide process. The fabrication process is finished by a two-level Al metallization. A scanning electron microscope (SEM) cross section of the emitter part of a transistor is depicted in Fig. 1.


Fig. 1. SEM of a TEMIC SiGe HBT.

This SiGe technology—based on a low-cost Si BJT technology ($f_T = 18$ GHz)—requires in its basic version only 16 mask steps, and provides the designer with n-p-n-SiGe HBT's, three resistor layers with different sheet resistivity, and spiral inductors. Due to the higher substrate resistivity of bipolar processes ($20\Omega \cdot$ cm) in comparison to CMOS and BiCMOS, the $Q$ factors of the inductors reach values which make them suitable for on-chip matching networks at 2 GHz [2]. An additional mask step (optional) provides the SIC transistor for very high-speed applications described above. Two optional mask steps provide the designer with nitride capacitors of high specific capacitance (1 fF/$\mu$m$^2$). These capacitors—adapted from monolithic microwave integrated circuit (MMIC) technology—are ideal for frequencies up to several gigahertz, allowing an additional degree of freedom for the designer, as there is no need for dc coupling of the transistors.

The solid curves in Fig. 2 show a typical Gummel plot of an HBT having the minimum emitter size of $0.8 \times 1.6$ $\mu$m$^2$ effectively. (The insert shows the location of the transistor on the wafer.) In order to estimate the ability to high-level integration, arrays of 10 000 HBT's (10K arrays) have been designed, each of these 10K arrays covering an area of about $1.5 \times 1.9$ mm$^2$. The dashed curves in Fig. 2 show a Gummel plot of the 10K array.

All 10K arrays accessible on a wafer have been measured. The results are compiled in Fig. 3, showing a wafer mapping of Gummel plots at $V_{CB} = 2$ V. In both Figs. 2 and 3, currents are plotted in a logarithmic scale ranging from 10 pA to 100 mA against $V_{BE}$ ranging from 0.2 to 1 V.

This result proves the quality of the technology and demonstrates the feasibility of medium-scale integration of SiGe HBT's with 20% germanium content in the base.

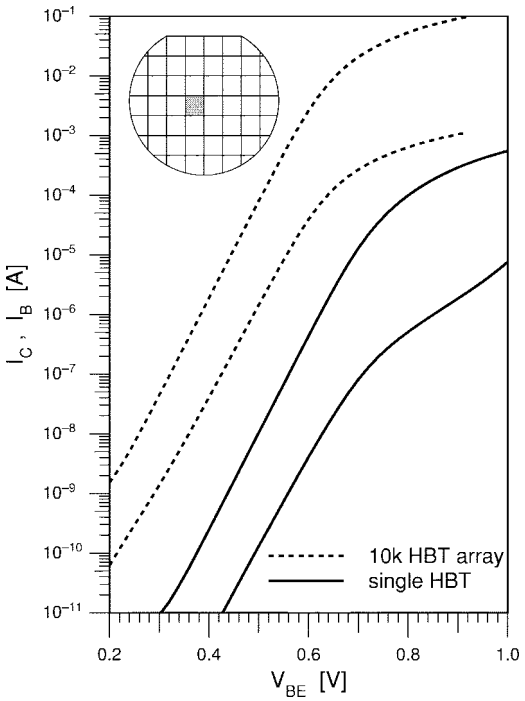


Fig. 2. Gummel plot of a single HBT compared to a 10-k HBT array (at $V_{CB} = 2$ V).

TABLE II
KEY PARAMETERS OF TEMIC'S SIGE TECHNOLOGY

| TEMIC-SiGe | with SIC | no SIC |
|---|---|---|
| $f_T$ | 50 GHz | 30 GHz |
| $f_{max}$ | 50 GHz | 55 GHz |
| $BV_{CE0}$ | 3.5 V | 6.0V |
| $F_{min}$ @ 2 GHz | 1dB | 1dB |
| 1/f corner freq. | 1kHz | 1kHz |

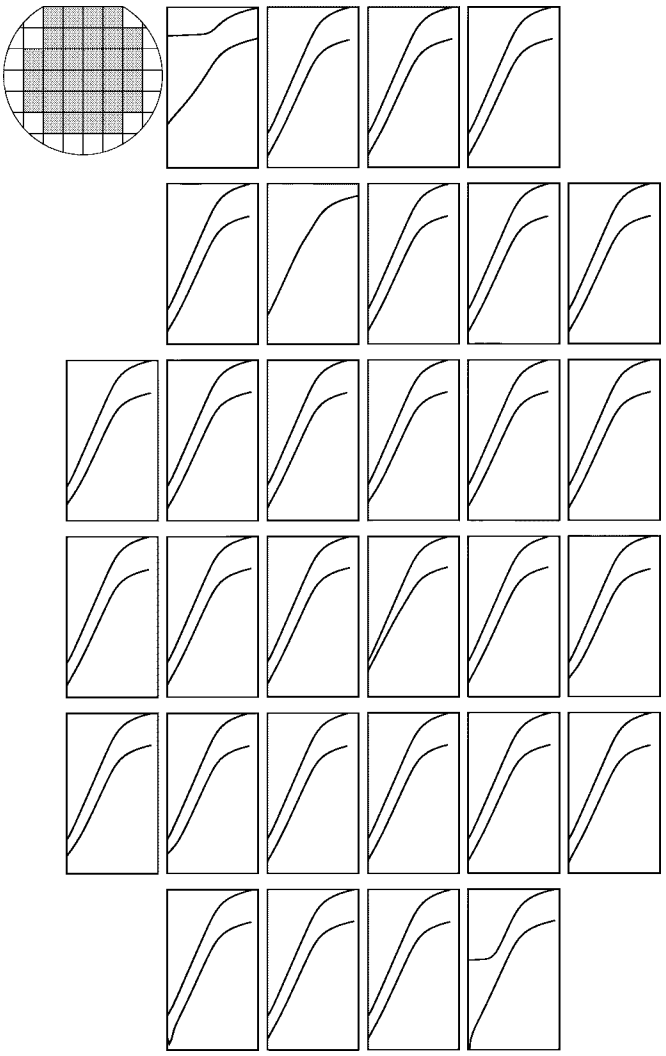

Fig. 3. Gummel plot wafer mapping of 10K HBT arrays at $V_{CB} = 2$ V.

Low-frequency noise measurements exhibited $1/f$ corner frequencies in the range of 1 kHz, and RF noise figures are well below 1 dB at 2 GHz. The measured transistor parameters are summarized in Table II.

## IV. LNA DESIGN

Based on the described process, a LNA has been designed for 1.9 GHz. The schematic is shown in Fig. 4.

The cascode arrangement eliminates the miller multiplication of the base–collector capacitance of the first transistor and makes the amplifier unilateral (low $s_{12}$) [7], [8]. This is a prerequisite of many communication systems to prevent leakage of LO power from the mixer back to the antenna. The optimum collector current level of the first transistor with respect to a minimum noise figure has been calculated using the method described in [1]. Simultaneous input and noise matching was achieved [7], [9] by a spiral inductor in the emitter lead of value

$$L \approx \frac{50\Omega}{2 \cdot \pi \cdot f_T} \tag{1}$$

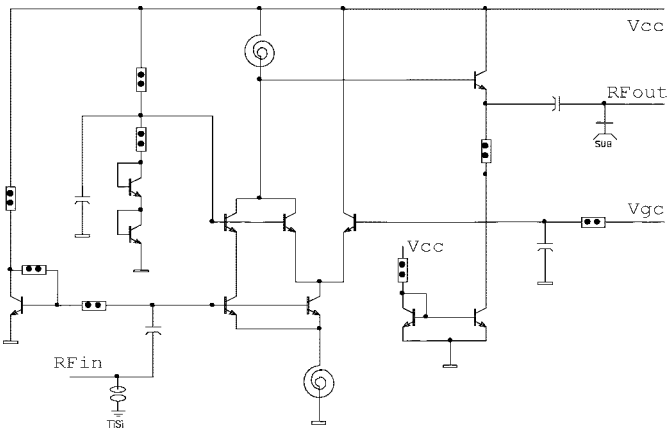


Fig. 4. Schematic of the 1.9-GHz cascode SiGe LNA.

where $f_T$ is the transit frequency of the device, as the input stage of an LNA is biased at a small current density to keep the noise figure low. Equation (1) clearly shows the need for high $f_T$ of the devices already at low current densities. The higher $f_T$, the lower the value of the inductor needed

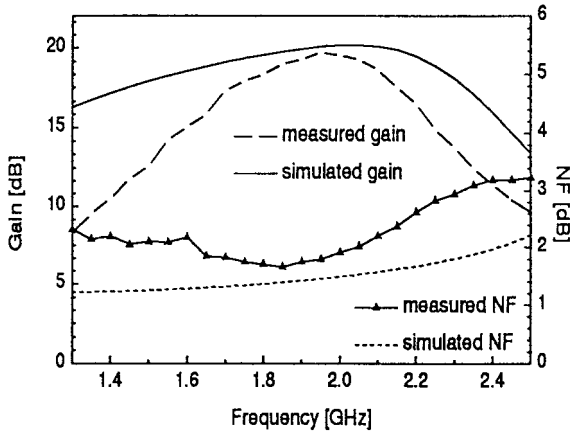


Fig. 5. Simulation and measurement results of the LNA. At 2.7 V, the LNA provides a gain of 20 dB with 1.8-dB noise figure and 9-dB input return loss.

for matching, and the lower the amount of noise added to the LNA by the series resistance of the spiral inductor. The capacitive feedback in the common base transistor is optimized for linearity, gain, and stability performance. To achieve gain control without sacrificing large-signal behavior, in the "low gain" operation mode, the gain control transistor shorts part of the RF power to analog ground $(V_{CC})$, whereas it is reverse biased and shut off in the "high gain" operation mode [10]. In the output stage of the cascode, a spiral inductor separates the RF from $V_{CC}$. The real part of the high-output impedance of the cascode stage is matched to 50 $\Omega$ by an emitter follower, the imaginary part by a nitride capacitor. To stabilize bias, a current source has been used for the emitter follower as usual. For the input stage, such a current source is prohibitive, as this increases the noise figure drastically. Therefore, a voltage source has been used to fix $V_{BE}$ of the input stage, increasing the noise figure only by about 0.25 dB in comparison to an ideal current source. A special low-noise pad structure is used at the input [11], contributing less than 0.1 dB to the noise figure of the LNA. Fig. 5 shows the simulation results. With a 2.7-V supply, the internally matched LNA provides a gain of 20 dB with 1.5-dB noise figure and 9-dB input return loss simulated in an SSO-20 package.

## V. PA Design

The thermal conductivity of silicon is three times higher as compared to GaAs, making silicon an ideal substrate material for PA applications. Load–pull measurements on SiGe HBT's have shown power-added efficiencies (PAE's) up to 44% in class A and up to 72% in class AB operation [12]. Encouraged by this, a SiGe HBT PA for mobile communication systems has been developed.

Fig. 6 shows a circuit schematic of the PA. It consists of a two-stage PA with an external output-matching network. The input matching is realized on chip. The first- and second-stage SiGe HBT's contain 10 and 60 emitter finger devices. They are biased at class A and class AB, respectively. To achieve high PAE, the emitter inductances of bond wires and package have to be kept as low as possible. The optimum load and source

Fig. 6. Schematic of the SiGe PA.

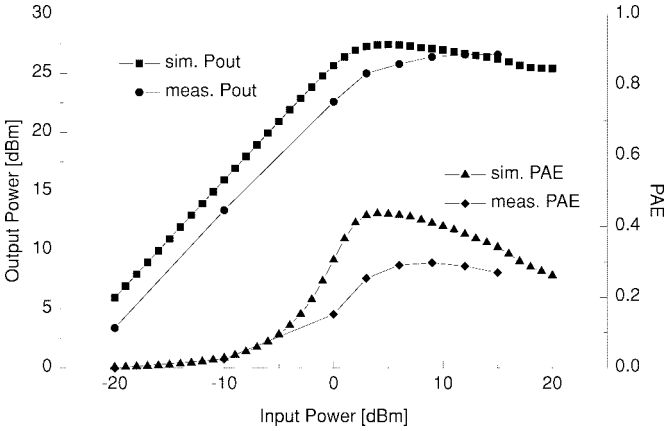


Fig. 7. Simulated and measured output versus input power and PAE of the DECT SiGe PA.

impedance of the PA are calculated with harmonic-balance simulation using load–pull measurements.

The results of the simulations are presented in Fig. 7. The simulated linear gain is about 26 dB. The maximum output power is more than +27 dBm and the maximum PAE at a supply voltage of 3 V is 45% @ 3-dB compression. The output power can be controlled by changing the control voltage from 3 to 0 V. Since the leakage current at $V_{\mathrm{ctrl}} = 0$ V is less than 1 $\mu$A, this amplifier is very useful for time-division multiple-access (TDMA) systems because expensive supply voltage switching (normally external MOSFET's or p-n-p transistors), which is needed in GaAs designs, is not required. The measurements are also shown in Fig. 7.

Also, a three-stage PA was designed. The first stage is realized by a four-emitter finger device which contains a negative feedback and an attenuator for stable operation and to keep VSWR low under large-signal conditions. The achieved linear gain is 30 dB, so just 0-dBm input power is needed to reach the compression point.

Optimization of PAE in PA's is required to increase the talk time in mobil communication systems. Because linearity in Gaussian frequency-shift keying (GFSK) modulation systems like digital enhanced cordless telecommunications (DECT) is not a problem, it is possible to operate in nonlinear amplifier

Fig. 8. Output matching network for class $F$ PA's at 1.9 GHz.

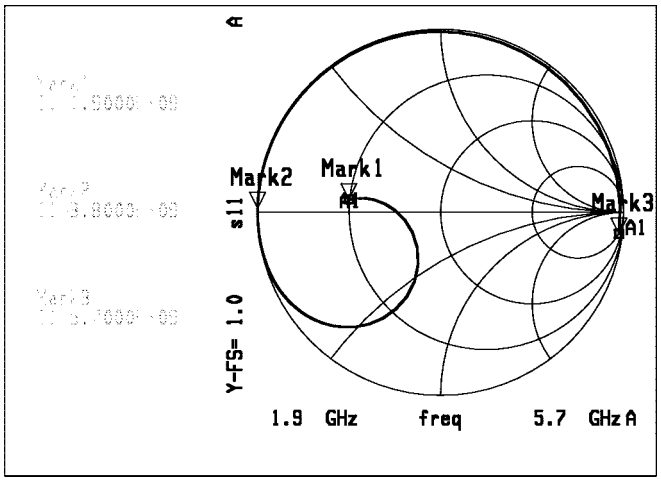


Fig. 9. Input impedance of the matching network for class $F$ PA's versus the frequency.

classes. A typical output network for class $F$ operation at 1.9 GHz is shown in Fig. 8.

The fundamental frequency is transformed from low impedance $(\sim 8\ \Omega)$ to 50 $\Omega$. The second harmonic is shorted, while in the case of the third harmonic, the 50-$\Omega$ termination is transformed to an open circuit. Fig. 9 presents the input impedance of a class $F$ matching network in a Smith Chart.

Harmonic tuning is a way to increase PAE [13], which requires active devices with a high transit frequency $f_T$. Thus, the PAE of SiGe HBT PA's as compared to ordinary silicon PA is higher or, in other words, the operating frequency can be up to two times higher at equal PAE in SiGe technology.

Fig. 10 shows the layout of an SiGe front-end including the two-stage PA and the LNA for TDMA systems at 1.9 GHz.

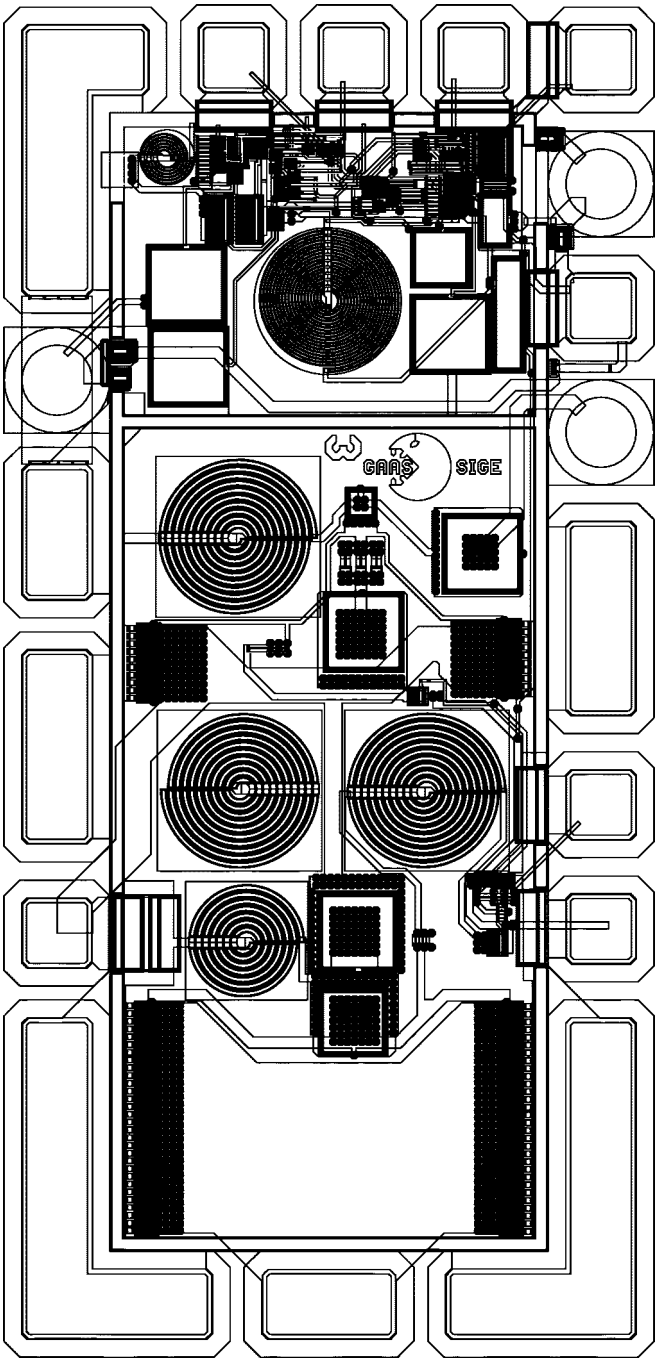


Fig. 10. Layout of the SiGe front-end. First measurements show a linar gain of 23.5 dB and $P_{\rm out}$ of 27 dBm at 1.89 GHz and a noise figure of 1.8 dB for the LNA.

## VI. Measurements of the Front-End

The front-end is designed in a small-size SSOP-20 package. In this package, the amplifier works with duty cycles up to 30% (sufficient for DECT handhelds and slow-hopping base stations). If a higher duty cycle is required, a P-SSOP-20 package can be used to provide sufficient thermal conductivity.

According to first measurements, the PA in class AB provides a linear gain of 23.5 dB and $P_{\rm out}$ of 26.5 dBm with a PAE of 30% at 1.89 GHz. The second and third harmonics are suppressed by more that $-30$ dBc and the intermodulation products are in DECT specification. In standby mode, the measured current consumption of the PA is just 0.1 $\mu$A, which makes it perfect for use in mobile communication systems. The difference of simulated and measured PAE is caused by a poor power distribution (too-low emitter resistors) and a nonoptimized output matching network.

In the next design step, higher emitter resistors for each transistor finger of the power devices have to be added to guarantee homogeneous power distribution. The resistor value has to be optimized $(R_E = 2\ \Omega, \cdots, 6\ \Omega)$ by load–pull measurements to find the optimum between maximum PAE and output power. Also, a class $F$ output matching network is currently under optimization to achieve more PAE.

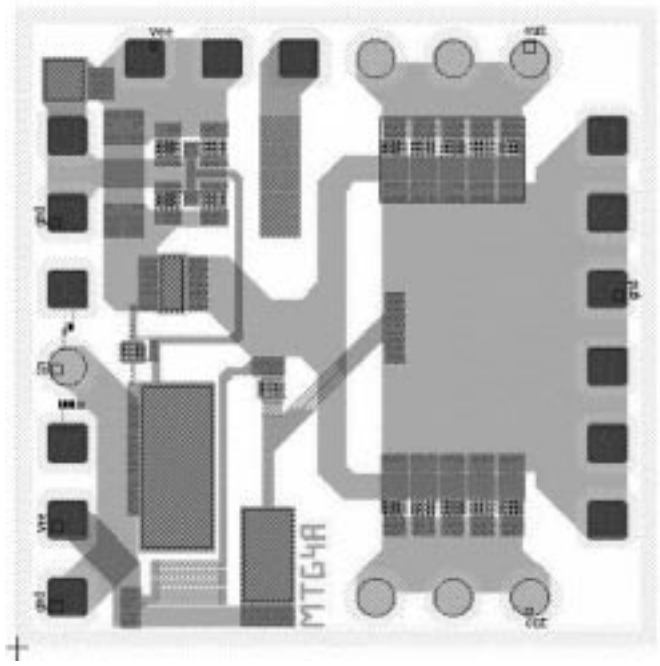

Fig. 11. Layout of the 900-MHz buffer amplifier.

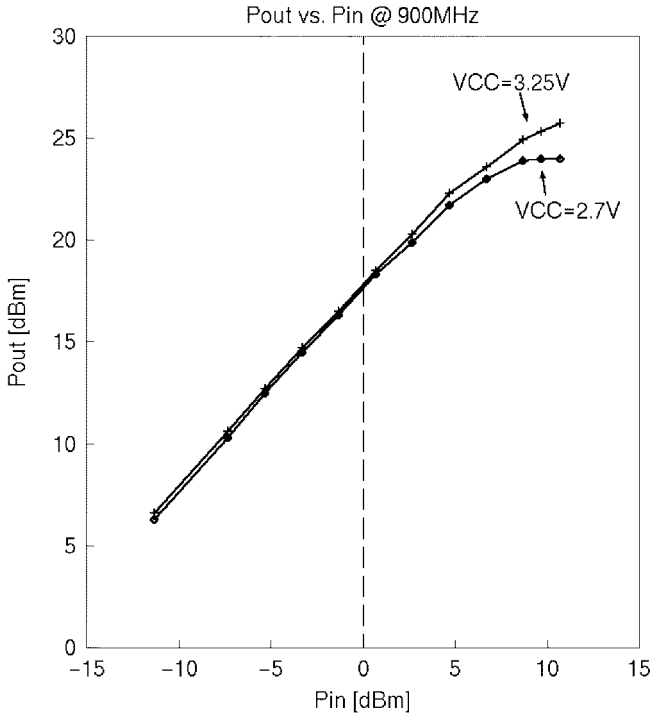


Fig. 12. Measured output versus input power of the GSM buffer amplifier.

The measurement of the LNA (see Fig. 5) shows that the simulated gain of 20 dB can be reached. The bandwidth of the LNA is smaller than simulated. This is due to the fact that the inductor at the output of the cascode forms a resonant circuit, in which the $Q$ factor of the spiral inductor is not modeled exactly.

The measured noise figure is about 1.8 dB at 1.9 GHz. This agrees well with the simulated value of 1.6 dB, which only accounts for device parasitics, but not for layout parasitics.

## VII. Global System for Mobile Communcation Pre-PA

In order to prove the performance enhancement employing SiGe HBT's for RF power applications over other competing technologies such as Si MOSFET, lateral diffusion MOS (LDD-MOS), GaAs HBT and GaAs MESFET, a buffer amplifier (BUFFER) for global system for mobile communication (GSM) has been developed and realized. This circuit shall be operated in front of the PA in the GSM-system architecture. The specifications for the output power are, therefore, somewhat moderate compared to the PA, but 27 dBm over the operating range still have to be achieved. Moreover, with the desired low-voltage operation, the supply voltage should be less than 3.6 V.

Fig. 11 shows the layout of the two-stage integrated circuit. The IC with the area below 2.5 mm$^2$ was bonded into a plastic SSO-20 package. Due to the high-$Q$ on-chip inductances and capacitances, parts of the matching and interfacing filters could be realized on the integrated circuit. The external matching network on the FR-4 PCB consisted of low-cost surface-mount device (SMD) components. These components were chosen with respect to low parasitics, high-power capability, and, of course, the dominant cost issues.

The first and second stage of the amplifier consist of distributed four and ten five-emitter finger devices, respectively. This device was choosen because of the good device performance and, moreover, design simulation versus measurement accuracy. In the simulations, all on- and off-chip parasitics have to be taken into account. Special care has to be taken of layout performance and succeeding layout parameter extraction. Furthermore, bond wires and package inductances have to be kept as low as possible and a special remark is put on chip packaging.

The measurement results of output power versus input power are shown in Fig. 12. The characterization was performed in an SSO-20 package mounted on PCB. A single supply voltage ranging from 2.7 to 3.6 V can be used. Maximum operation condition is 5.5 V. The measured output power was up to 27 dBm with a gain of 17 dB as simulated. Low second- and third-order harmonics were found around −40 dBc. The PAE was measured above 35%.

In a new approach with a slightly bigger chip size (which is currently in fabrication), the above demonstrated that achieved values could be increased, therefore, emphasizing the suitability of this technology for RF power applications even more. Simulation results forecast values for maximum output $P_{\text{out}}$ of around 29 dBm with a PAE reaching 50%.

## VIII. Conclusion

We reported on design aspects and the implementation of RF IC's using TEMIC's SiGe heterojunction bipolar technology. The differences between the device parameters of Si BJT and SiGe HBT technology and their influence on IC design have been discussed. The simulations and measurements show the great potential of this technology for the realization of RF integrated circuits (RFIC's), e.g., for front-end applications in mobile communication systems.

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In 1995, he was a Visiting Researcher at the University of California at Los Angeles, where he was engaged in design of microwave circuits. In 1996, he joined the Daimler-Benz AG Research Center, Ulm, Germany, where he worked in the design and development of integrated microwave circuits. Since October 1996, he has been with TEMIC Semiconductor GmbH, Heilbronn, Germany, and is active in the design of SiGe HBT circuits for mobil communication systems.

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From 1993 to 1996, he was with the Daimler-Benz Research Center, Ulm, Germany, where his research activities focused on SiGe MMIC technology on high-resistivity silicon substrates and MMIC design. In 1997, he transfered to the Development Department, TEMIC Semiconductor GmbH, Heilbronn, Germany, where he concentrates on RFIC design for communication circuits using TEMIC's SiGe bipolar process.

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